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Test Strategies for NASAs 3-D Stack Multichip Module Space Flight Computer

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Abstract

Advanced packaging technologies such as 3D chip stacking, multichip modules (MCMs), and 3D stacks of MCMs provide opportunities for significant reductions in system mass, volume and power. They also pose major testing challenges that need to be resolved before they are used in mainstream designs. Among these challenges, the problems of achieving acceptable assembly yields and meeting product quality requirements through appropriate test methodologies are very critical. Both these problems can be significantly alleviated by adopting testing approaches which guarantee the integrity and performance of the underlying packaging technologies. In this paper, we propose test methodologies for a 3D stack of MCMs used by the flight computer of the NASA New Millennium Program (NMP) Deep-Space mission spacecraft. The test methodologies are based on the IEEE 1149.1 Boundary Scan Standard architecture. Special test chips are used for reliable test and diagnosis of the 3D MCM stack-based flight computer architecture. Also, the range of test options available are evaluated and ranked with respect to test time, test hardware, number of test lines, and test reliability. The test hardware has been fabricated and is scheduled to fly in space in the near future.

1 Introduction

Advanced microelectronics packaging technologies such as multi-chip modules (MCMs), 3D chip stacking, and MCM stacking are being used by NASAs New Millenium Program (NMP) to develop a highly integrated 3D microavionics architecture for future space science applications. The flight computer currently under development for the NMP Deep Space-1 mission, consists of a 3D stack of MCMs that includes the functionality of the spacecraft flight computer, large local memory, non-volatile memory, and a high bandwidth I/O interface [1, 2]. This set of modules is expected to weigh about 1.5 kg, which represents more than an order of magnitude reduction in spacecraft mass relative to the state of the art. This will enable frequent, low cost, miniature scientific missions to the outer planets. Figure 1 depicts the 3D MCM stack approach.

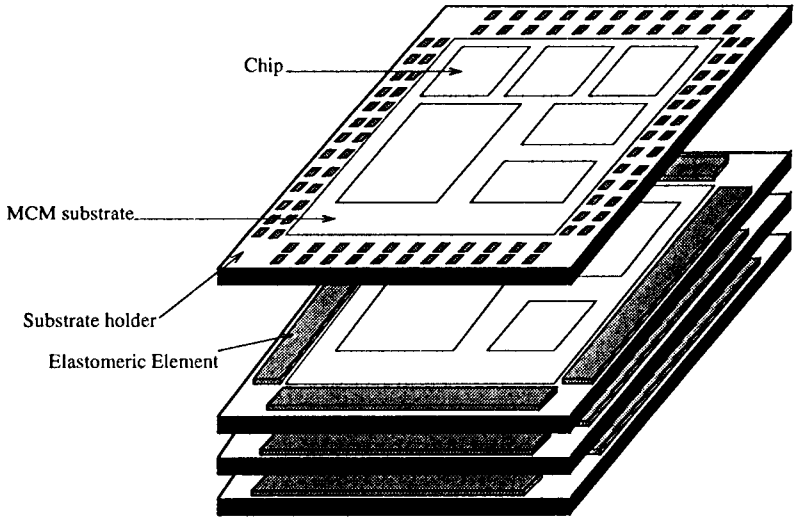

Figure 1: 3D MCM Stack

The processor module (one slice of the stack), designed by Lockheed Martin Federal Systems, consists of the RAD6000-5L processor, the Local Input Output (LIO) chip, oscillators and Start Up ROM (SUROM) [2]. The second module contains 400 Mbytes of local memory implemented using five 40-high 3D memory cubes of 16 megabit DRAM chips. The non-volatile memory module, designed by TRW, has a total of 1 Gbits of flash memory, using 32 Mbits plastic-packaged parts stacked four high. Finally, the I/O module, designed by Boeing, includes the

following interface logic: A PCI bus for inter-module communication, fiber optic I/O bus, and a PCI bus to VME bus bridge for communication with the rest of the spacecraft. All the four modules are packaged together using a low cost, flexible MCM stacking technology developed by SCC and being integrated at the NASA Jet Propulsion Laboratory (JPL). The MCMs are mounted on printed circuit boards (PCBs), which are then stacked in three dimensions, using elastomeric interconnects. The 3D MCM space flight computer will undergo exhaustive testing and diagnosis at JPL before integration into the spacecraft. The block diagram of the computer is shown in Figure 2.

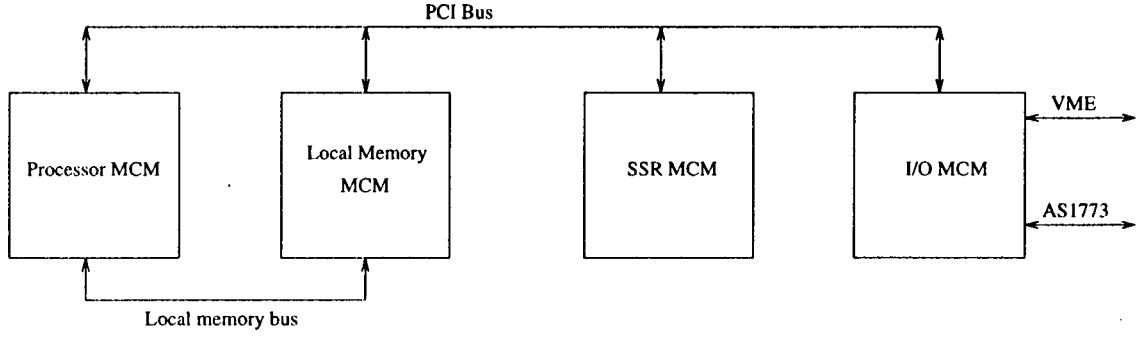

Figure 2: 3D microavionics stack block diagram.

Among the many issues that need to be resolved before the MCM stack is fabricated, validated and inserted into the space missions of the 21st century, is the problem of electrical and functional testing of the assembled MCM stack. This involves extensive boundary scan based testing, wherein each MCM slice is tested separately and also as part of the assembled package.

The IEEE Standard 1149.1 Boundary Scan Architecture [4] is used widely to facilitate the testing of MCMs. The boundary scan architecture associates a memory cell with each I/O pin of a chip. These memory cells (or boundary-scan/BS cells) are connected in series to form a shift register, called the boundary scan (BS) register. The test standard contains a four port connection, the Test Access Port (TAP). The TAP consists of four lines, namely the test clock (TCK), test mode select (TMS), test data in (TDI) and test data out (TDO) lines. Test instructions and data are sent over the TDI line. The test results are transferred to the external tester over the TDO line. The signal TCK carries the test clock. The state of the test circuitry in the associated chip is defined by state transitions on the TMS line which are decoded by the

TAP controller (TAP CTRL in Figure 3). The test architecture and implementation details are described in [4]. Figure 3 shows the general test architecture of a chip which supports the boundary scan standard.

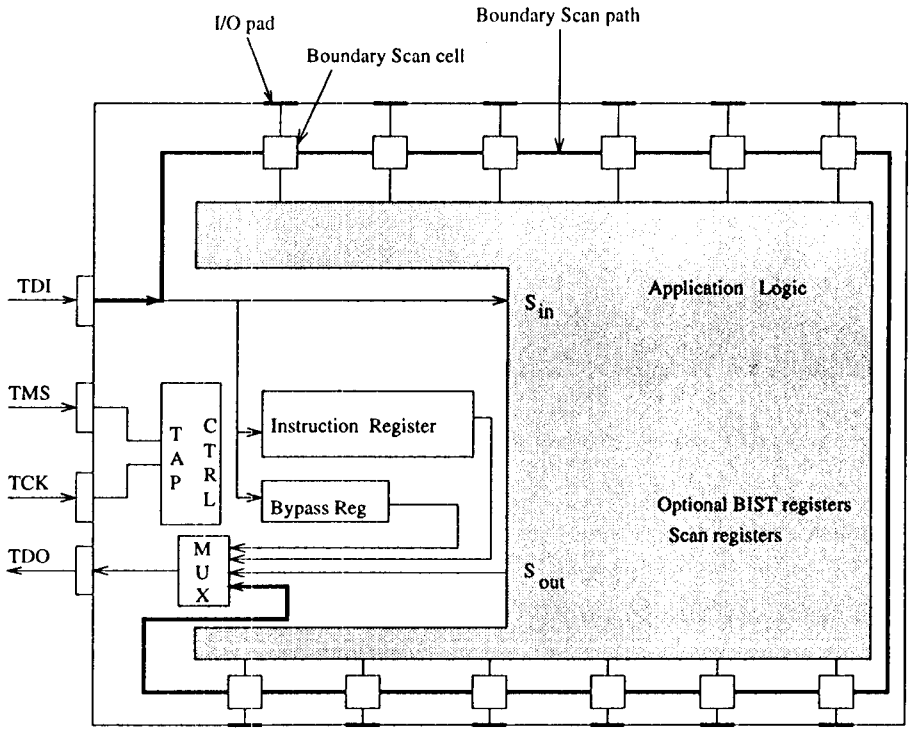

Figure 3: Chip supporting boundary scan standard IEEE 1149.1.

In the past, several techniques have been proposed for testing multi-chip modules. The structured testability approach for MCMs based on built-in self-test (BIST) and boundary scan, proposed in [3] is well-accepted in industry. This approach is based on implementing die level BIST (BIST is a design for testability technique that allows a circuit to test itself and is typically used to detect stuck-at faults in the application logic of the associated die) and module-level boundary scan in the MCM design (Figure 4).

For test purposes, the BS cells of all dies in an MCM are connected into one single scan path, where the TDO of one die is tied to the TDI of another die, except for the initial TDI and last TDO ports which are tied to the distinct terminals of the MCM (Figure 4). Using this configuration, various tests can be carried out, including (1) interconnect test, (2) snapshot observation of the normal system data, and (3) testing of each chip [3]. To enable (3), special

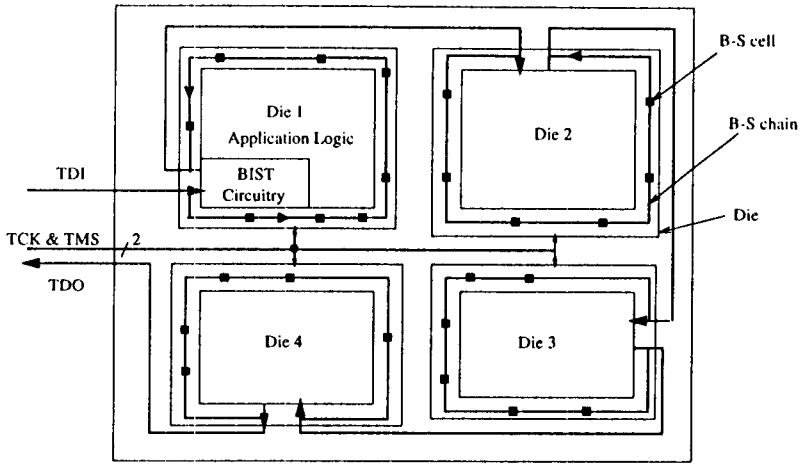

Figure 4: Boundary Scan in an MCM.

special test instruction are sent to a desired die, through the boundary scan path, to activate its BIST hardware. The results of the BIST process can then be observed, through the boundary scan signals, to determine if the die is "good" or "bad".

In this paper, we describe test methodologies for 3D MCM stacks under the assumption that the integrated circuits (ICs) in each slice of the stack are compatible with the IEEE JTAG 1149.1 boundary scan standard and that they are equipped with built-in self-test mechanisms that can be activated under JTAG control. The goal is (a) to test all the interconnections between the ICs of each slice of the 3D stack, both within each slice as well as across slices and (b) to activate the internal self-test mechanisms (BIST) of each IC under JTAG control. This validates the functionality of each IC as well as the interconnections between all the ICs incorporated into the 3D MCM stack, providing comprehensive test of the stack electronics. The design of the test hardware is motivated by the need to test the stack electronics reliably in the presence of faults in the boundary scan circuitry, such as an open TDI line. Of particular concern are faults that can render the entire 3D stack untestable. Hence, the proposed test methodologies are also evaluated in the context of test reliability, that is, the ability to test the 3D stack in the presence of point failures in the test hardware itself. It is also desired that the test architecture employed be scalable; i.e. enable the addition of stack slices without any change in the test methodology. Further, the test time necessary for testing an embedded IC must depend only on the test sequence length for the IC and not on the number of ICs in the

3D stack or the test complexities of other embedded ICs. In general, due to the involvement of different industrial partners in the manufacture of each slice of NASAs 3D MCM stack, it is also necessary to have an "open and pluggable" test architecture that allows seamless testing across different slice technologies. Finally, a key design goal is to ensure that the same test approach is used to test the 3D stack in flight as on the ground.

The remainder of this paper is organized as follows. In Section 2, test strategies based on different boundary scan bus configurations are described. In Section 3, test techniques based on inclusion of an MCM test controller chip in each 3D MCM slice is discussed. In Section 4, a robust built in self test (BIST) approach for the stack is developed. The various test techniques are comparatively evaluated in Section 5. The test architecture incorporated in NASAs space flight computer module is described in Section 6. Finally, a description of the test sequence employed to test the space flight computer module is presented in Section 7, followed by conclusions.

2 Test Strategies Based on Specialized BS Bus Configurations

In this section, we present three simple strategies for testing a 3D stack of MCMs. Each strategy is characterized by an associated test bus configuration and a number of test lines. It is assumed that no special test chips are included in the MCM slices. The pros and cons of each approach are also briefly described.

2.1 Serial Module Scan Test

This strategy is a direct extension of the approach proposed in [4] for testing multiple chips on a board. In this technique, the boundary scan registers in the ICs of the MCM slices are connected in a single serial scan chain running through the 3D stack as shown in Figure 5. The test data is distributed to all the MCM slices through the TDI input of module 1 which is connected to the external tester (every module shown in the figure corresponds to a slice of the 3D MCM stack). Further, the test responses from all the slices are scanned into the external

tester through the TDO line of module 4 (slice 4). The TMS and TCK lines are fed in parallel, to all the slices. The above test configuration has several drawbacks which are discussed below.

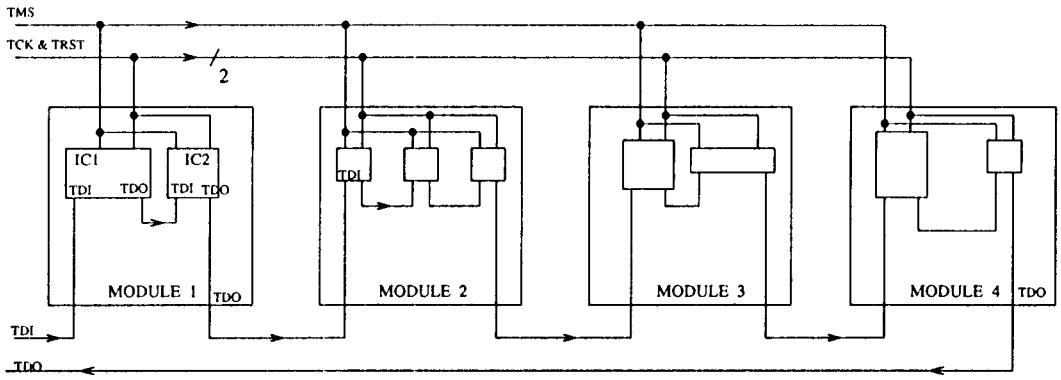

Figure 5: Serial Module Scan Test

1) The test approach is not very reliable as a fault in the boundary scan chain between two ICs can prevent the entire stack from being tested.

2) The time needed to test an MCM slice individually is dependent on the complexity of other slices in the 3D stack. During the test of a single MCM slice, the boundary scan (BS) hardware in other slices is placed in BYPASS mode. A chip is in BYPASS mode when a single flip flop is connected between the TDI and TDO lines of its boundary scan hardware. An entire slice of the 3D stack can be placed in BYPASS mode by placing all its ICs in BYPASS mode. In this mode of operation, the number of flip-flops connected between the TDI and TDO lines of the concerned slice is equal to the number of ICs connected in the boundary scan chain within the slice. As an example, in Figure 5, when module 1 (slice 1) is tested, there are seven flip flops connected in the serial chain between the TDO line of module 1 and the TDO line of module 4 (slice 4). This adds a delay of seven clocks for every test vector applied to slice 1 and is substantial when the number of test vectors applied and the number of ICs in other slices is large.

3) It is not possible to test a slice without knowing the test architecture of the other slices (the number of chips to be placed in BYPASS mode and the delay incurred in scanning test data must be known).

4) During test of a single MCM slice, other slices in the stack must be powered up to enable all of them to be in BYPASS mode.

There are two advantages to this technique. Only four test lines are required to test the complete 3D stack. Further, no extra test hardware is needed at the MCM and 3D stack levels other than what is provided by the JTAG 1149.1 standard. In summary, however, the inability of the test process to withstand point failures in the BS bus and test hardware is of serious concern. In the following, we discuss BS test bus configurations that allow the 3D stack to be tested reliably in the presence of point failures.

2.2 Multiple Module Control Test

In this test approach, each slice has a separate TMS line associated with it, as shown in Figure 6. The TDI (TDO) lines from each slice of the 3D stack are connected directly to the external tester. Overall, seven test lines are required; TCK, TDI, TDO and four TMS lines (one connected to each slice).

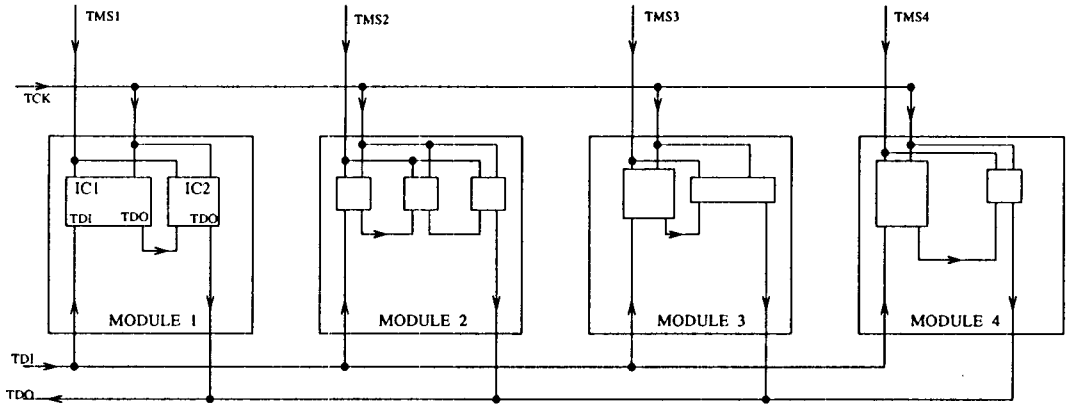

Figure 6: Multiple Module Control Test

The advantages of multiple module control test are given below:

1) Continuous boundary scan register chains are restricted to lie within a single 3D stack slice, unlike serial boundary scan test in which the chain spans multiple slices. Hence, test reliability is improved as most faults in a slice do not prevent other slices from being tested.

2) Each MCM slice is tested independently. The test data for a slice is not transmitted

through other slices. The test data is scanned into the TDI line of a slice by placing the data on the TDI port of the 3D stack. Further, results are scanned out of the TDO line to the external tester directly. Hence, it is ensured that at any instant, test data is scanned out from only one MCM slice into the external tester.

3) An MCM slice can be tested in isolation without powering up other slices in the 3D stack. This is done by activating the TMS line connected to it while other TMS lines are held idle.

4) The structured test of an MCM involves module level interconnect test and IC level built in self test (BIST). The use of multiple TMS lines enables BIST and interconnect test to be performed in different slices simultaneously. For example, while slice 1 is subjected to interconnect test, it is possible to initiate BIST in the other slices before the start of interconnect test in slice 1. Hence, by suitably configuring the test operations, the test time for the 3D stack can be minimized.

Thus, this technique is more robust from a test perspetive, than the serial chain scan approach. However, faults on the TCK line will prevent the entire stackfrom being tested. Also, specific stuck-at faults on the TDI and TDO lines could be critical. Hence, in the next section, we present a parallel module test strategy where separate test buses are provided to each MCM slice in the 3D stack.

2.3 Parallel Module Test

In this approach, each slice has a separate TMS, TDI, TCK and TDO line associated with it (Figure 7). All the slices can be tested independently in parallel. This test approach is more reliable than the previous approaches as faults on the TCK line of a slice do not prevent other slices from being tested. Also, the slices can be tested at different clock frequencies unless the test procedure relies on synchronization between circuitry in different slices or the entire 3D stack assembly is being tested for reliability. This test approach provides maximum parallelism in test application and allows the test results for each slice to be analyzed independently. However, this technique requires the maximum number (12) of test lines, four to each slice.

All the test strategies presented in this section involve varying the number of test lines to increase test reliability, test speed and test parallelism. The number of test lines vary from a

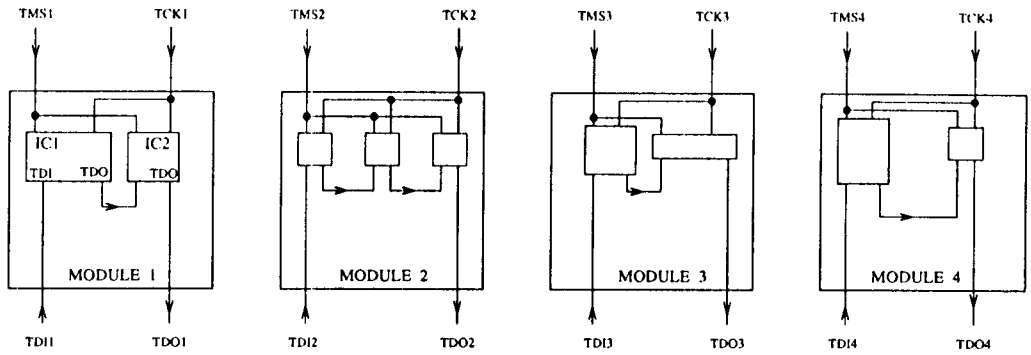

Figure 7: Parallel Module Test

minimum of 4 to a maximum of 16. No extra hardware is employed at the MCM and 3D stack levels. The choice of one of the above test approaches for a particular test application is driven by the number of test buses allowed by the external tester, the test parallelism allowed by the test software in the external tester and the number of pins provided for test in each slice and the MCM stack. In the following section, we discuss test strategies that incorporate a test die in each MCM slice for enhanced diagnosis and test reliability.

3 MCM Test Controller (MTC) Based Strategies

In this section, we present test techniques based on inclusion of a test controller die in each slice of the 3D stack. A MCM Test Controller (MTC) die is incorporated in each slice to control its scan path during test. The MTC includes a TAP controller and an optional boundary scan register through which test vectors are scanned in and applied to the non-BS dies [5, 6]. It has a single bit BYPASS register that enables an MCM slice to be considered as a single JTAG device and placed in BYPASS mode when necessary. This is depicted in Figure 8.

Further, the scan path itself can be reconfigured using a Scan Path Linker (SPL) [7, 8] to control the scan path configuration in an MCM (Figure 9). The Scan Path Linker partitions the scan path in an MCM into multiple secondary scan paths (SSPs). By scanning in a control word, the scan path linker selects one or more of the secondary scan paths and includes it in the primary scan path (PSP). This increases the reliability of the scan chain. For example, when the control word is 1010, chips 1 and 3 are connected in a chain. The TDI line is

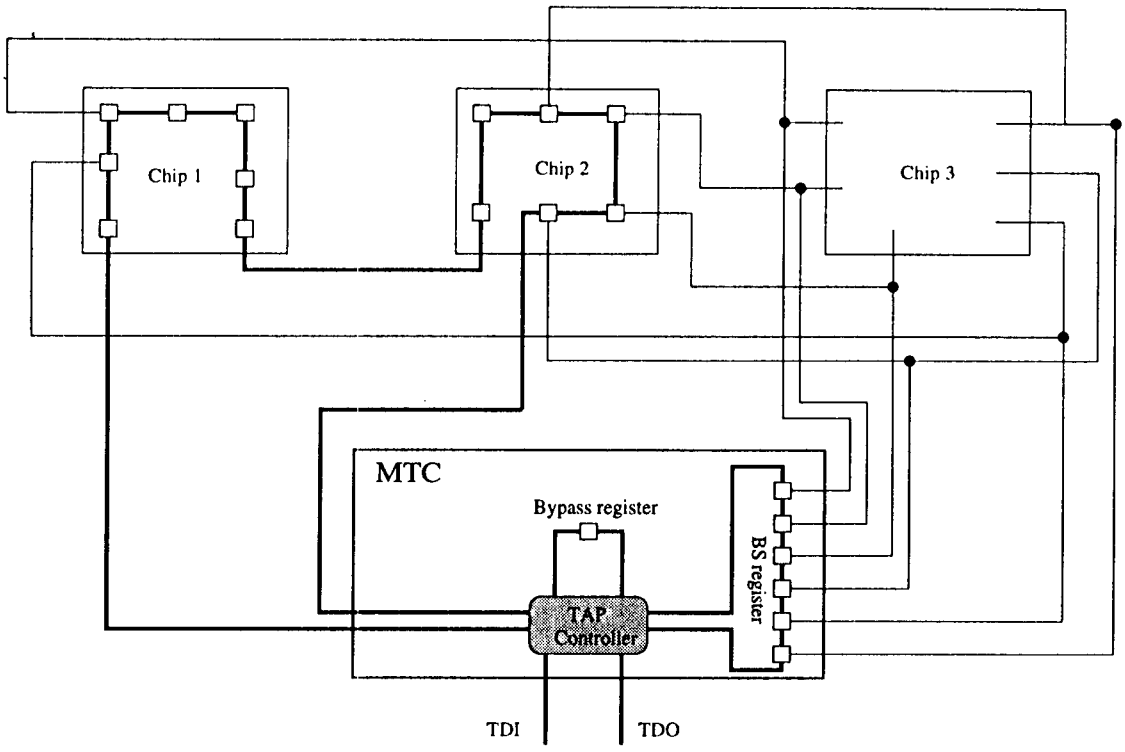

Figure 8: Test features included in MTC.

connected to TDO1, TDI1 is connected to TDO3 and TDI3 is connected to TDO. Faults in a particular section of the scan chain in an MCM are easily isolated without affecting the test operations in fault-free parts of the MCM. The test hardware required for the scan path linker is approximately 75 gates [7]. The proposed MTC architecture consists of 240 gates [9] and includes a TAP controller and boundary scan register as discussed earlier, as well as a scan path linker. We shall now briefly describe two strategies based on inclusion of the MTC in each slice and the test bus configurations described in the previous section.

The serial MTC based test technique (Figure 10), proposed in [8], is developed from the serial module scan test approach. An advantage of this technique over its parent scheme is that when an MCM slice is placed in BYPASS mode, only a one-bit register is placed between the external TDI and TDO lines of the MCM, irrespective of the number of chips connected in the scan path. A fault in the scan path between two slices will prevent test of the 3D stack. However, a fault in the scan path in a slice will not affect test of the other slices, as the MTC in the faulty slice is placed in BYPASS mode. Hence, this test technique is more reliable than

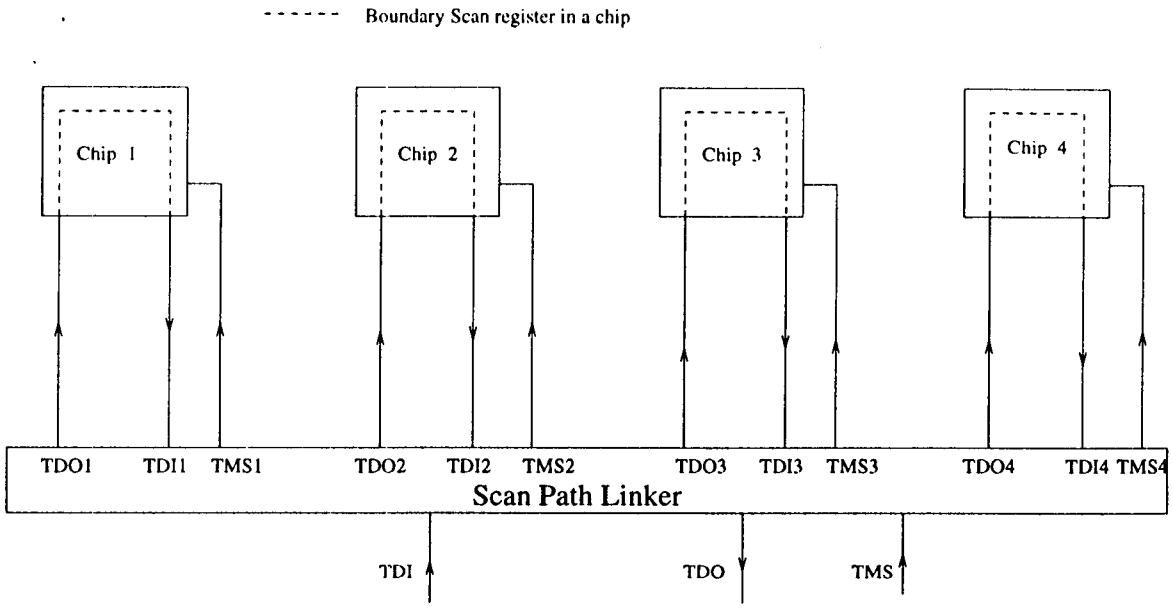

Figure 9: Scan Path Linker in an MCM.

serial module scan test.

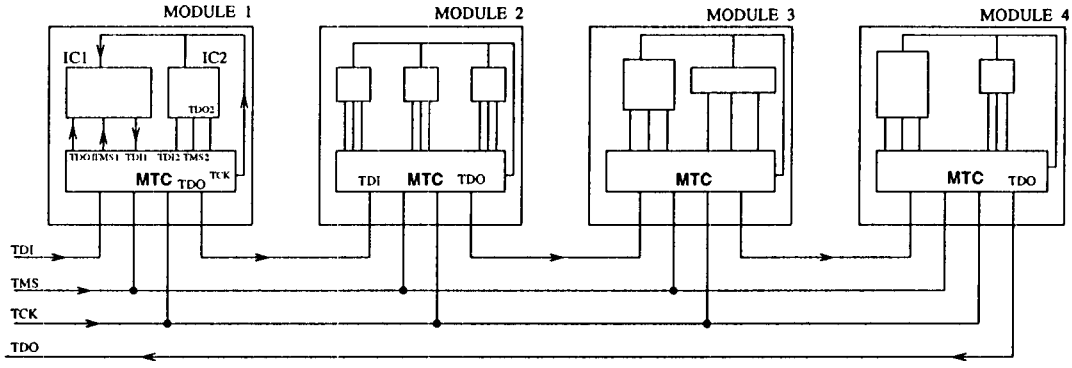

Figure 10: Serial MTC based Test

Similarly, techniques for incorporating MTCs into each slice for multiple module control test and parallel module test can be defined. The parallel MTC based test approach corresponds to the other end of the test spectrum with the maximum number of test lines and maximum additional test circuitry (Figure 11). It is also provides for a very reliable test methodology.

We have hereby identified techniques for off-line testing of a 3D stack after assembly, using an external tester. For space applications it is equally important to consider autonomous test

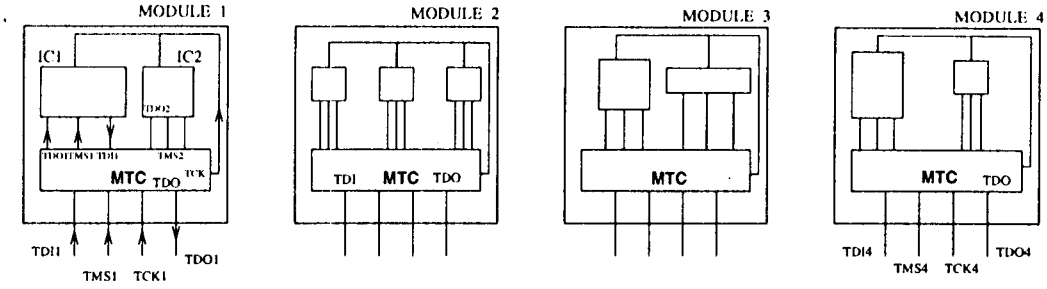

Figure 11: Parallel MTC based Test

of a 3D stack using built-in self-test (BIST) mechanisms that can be used in the absence of an external tester. To enable such BIST, a master test controller that manages the test process must be used. In the next section, we describe two test strategies that rely on the use of a master test controller for BIST of a 3D MCM stack.

4 Master MTC based Test

This test strategy identifies the MTC in slice 1 of the 3D stack as the Master MCM Test Controller (MMTC) (Figure 12). The MMTC controls flow of test data to the slices of the 3D stack. During assembly test, the MMTC is connected to an external tester through a single JTAG bus. Further, the MMTC is connected to the MTCs in other slices through separate JTAG buses. Thus, by sending a control word to the MMTC, the JTAG bus from the external tester is connected to one of the three buses that transfer test data to the slices of the 3D stack. The test hardware in an MMTC consists of 310 gates [9]. For purposes of autonomous test of the 3D stack, the MMTC contains an optional control and data buffer (CDB) that stores test data. This test data is loaded into the buffer after assembly of the flight computer module.

The test process for the 3D MCM stack proceeds as follows. First, self-test of the MMTC is enabled. Subsequently, the MMTC tests the JTAG buses connected to other slices and the other MTCs. Then the 3D stack slices are tested. A control word is initially sent to the MMTC to choose a slice to test. This connects the JTAG bus from the external tester to the appropriate slice through the MMTC. Subsequently, control words are sent to configure the scan chains in the slice (done by MTC). Test data is then scanned into the MCM slice.

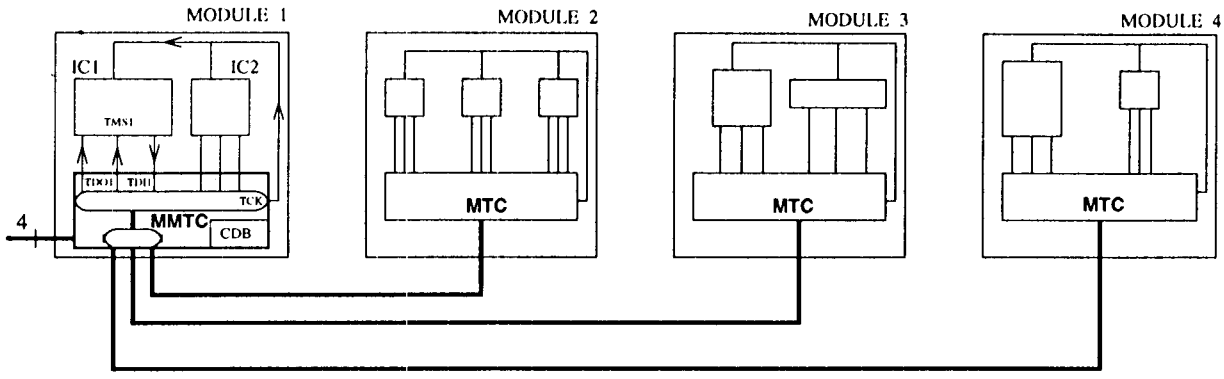

Figure 12: Master MTC based Test

The above technique permits BIST of a 3D stack by the MMTC. However, it is not very reliable as the 3D stack cannot be tested if the MMTC is faulty or if the JTAG bus between the external tester and MMTC fails. Also, if the JTAG bus connected between a slice and the MMTC fails, then the slice cannot be tested. In the next section, we propose a reconfigurable test technique that addresses some of these problems.

4.1 Reconfigurable MTC (RMTC) based Test

In this section, we propose a reconfigurable test technique that provides enhanced test reliability and BIST of a 3D stack of MCMs. Two features are provided in a 3D stack for test purposes: redundant test lines and a reconfigurable test architecture. The test ICs in all the slices are identical and are denoted as Reconfigurable MCM Test Controllers (RMTCs). One of the RMTCs is selected as the master test controller of the 3D stack. Further, redundant test lines are provided to enable test in the event that some of the lines are faulty. All the test lines are bidirectional and can be configured as input or output lines by the RMTCs.

The Boundary scan architecture requires a minimum of four test lines -TDI, TDO, TCK and TMS. In our approach, we provide additional test lines that are connected to the RMTCs as shown in Figure 13. The test bus is common to all the slices in the 3D stack. In the example shown, two extra redundant lines are provided.

Each RMTC contains the basic circuitry included in an MMTC (described earlier). It also contains circuitry to detect faulty test lines and configure the test bus appropriately. The test

hardware in a RMTC consists of 460 gates. Also, the RMTCs mutually test themselves. In this manner, they identify the fault-free RMTCs and vote one of them to function as the Master MCM Test Controller. Thus, the test of the 3D stack is not inhibited even when some test lines or RMTCs are faulty. The test architecture is described in detail in [9].

Initially, all the RMTCs perform self test in parallel. Subsequently, they mutually verify the response of the self test. Then one of the fault-free RMTCs is selected as the master. The master RMTC tests the JTAG bus and configures the test lines. Subsequently, the 3D stack slices are tested by their respective RMTCs.

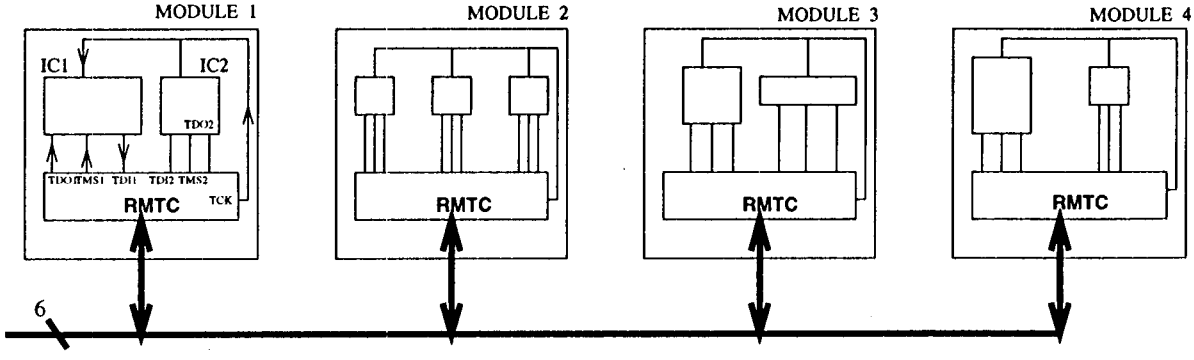

Figure 13: Reconfigurable MTC based Test

The test approach fails only when all RMTCs or all test lines in a 3D stack are faulty, which is highly improbable. Hence, this test approach is very reliable for a 3D stack of MCMs. Further, this technique is easily scalable to 3D stacks of MCMs of larger sizes. Additional slices can be added and connected to the test bus without any changes to the test architecture of the slices in the original stack.

5 Comparison of Test Strategies

In this paper, we have discussed seven test strategies for a 3D stack of MCMs. We shall now compare the approaches with respect to test hardware, test time, test lines, and test reliability. The number of MCM slices in a 3D stack is assumed to be N. The test scan chains in all the slices are assumed to be of the same length. The time taken to test a 3D stack using the serial

Test Strategy	Test Lines	Hardware (gates)	Test Time	Reliability
Serial Module Scan Test	4	-	T	1
Multiple Module Control Test	$4 + Log_2(N)$	-	$< T$	4
Parallel Module Test	4N	-	T/N	5
Serial MTC based Test	4	N × 240	T	2
Parallel MTC based Test	4N	N × 240	T/N	6
Master MTC based Test	4	310 + (N-1) × 240	T	3
Reconfigurable MTC based Test	4 + X	N × 460	T	7

Table 1: Comparison of the test strategies for a 3D stack of MCMs.

module test approach is denoted by T and is used as a reference for comparison. The results are presented in Table 1.

In Table 1, "test lines" refers to the number of lines that need to be connected from an external tester to the associated 3D MCM stack for test application. Further, "test hardware" refers to all the additional circuitry (circuitry in test ICs) incorporated in every slice of the 3D stack, for enhanced test of the stack. Note that since the additional logic required for test in each slice is not very large, this may be incorporated into any of the ICs in the MCM slice if there is flexibility to do so. Table 1 does not include the logic complexity of the TAP controller circuitry in every IC that is due to the JTAG boundary scan test standard. The test strategies are ranked from 1 to 7 with respect to test reliability, with 7 being the most reliable.

As explained in the previous sections, serial module scan is the least test reliable approach. The MTC based serial module test technique is more reliable but has some of the deficiencies of serial module scan test. The Master MTC based test technique is ranked 3 because faults in the MMTC are catastrophic and prevents test of the entire module. This is followed by the multiple module control and parallel module test strategies. The parallel MTC based test approach is the second most reliable technique and requires the maximum number of test lines. Finally, the reconfigurable test approach is the most reliable and requires the most complicated test hardware, i.e. the RMTCs.

The number of test lines needed for the reconfigurable test approach is variable and depends on the availability of test pins on the the 3D stack. X refers to the number of extra test lines required by the technique.

The test time is minimum for parallel test strategies as the MCM slices in the associated 3D stack are tested in parallel. However, they approaches require the most number of test lines, four lines from the external tester to each MCM slice.

In the following, we discuss the test architecture incorporated in NASAs 3D microavionics stack.

6 Test Architecture of NASAs Deep Space Microavionics Stack

The test strategy implemented for NASAs 3D microavionics stack incorporates specific features included in the multiple module control test technique discussed earlier, with additional redundant test lines. This approach was chosen over the MTC based test strategies, due to practical difficulties in procuring radiation-hardened (rad-hard) RMTC IC implementations, a requirement for deep space mission electronics. It is expected that in the future, such rad-hard ICs will become available.

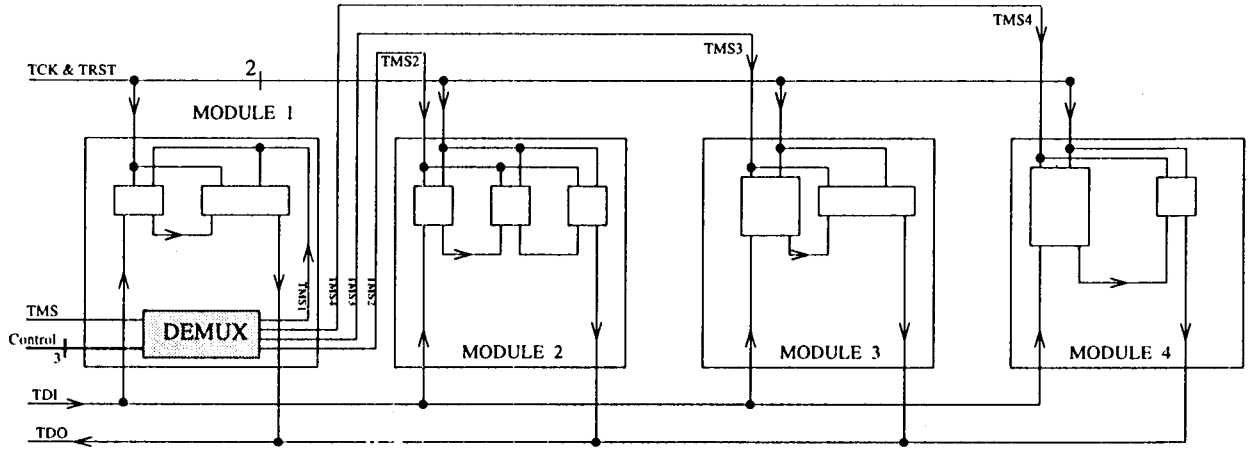

Figure 14: Test Scheme for 3D flight computer module

Each MCM slice in the 3D stack has a separate TMS line associated with it. However, there

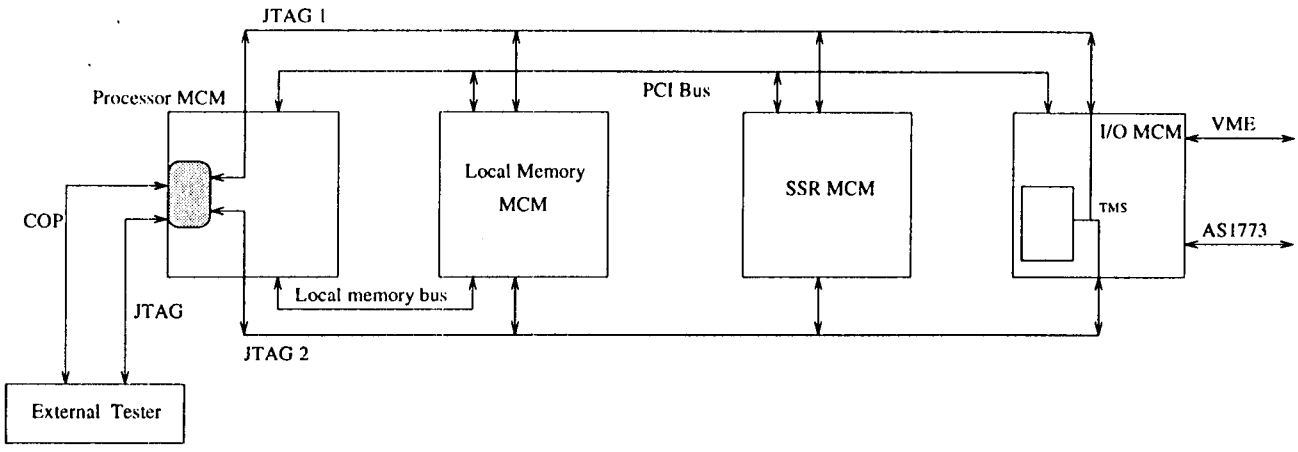

Figure 15: Redundant JTAG Buses in the 3D MCM stack.

is only one TMS line that is connected to the microavionics stack from the external tester. A 4:1 demultiplexer is used to connect the external TMS line to one of the TMS lines corresponding to the different slices. This is shown in Figure 14.

In order to allow test of the 3D stack in the presence of specific failures in the test lines such as line opens, a pair of redundant buses running vertically along opposite sides of the stack and feeding each MCM slice, is provided. The two buses are connected in "wired-OR' configuration at their destination terminals in each slice of the 3D stack. This is shown in Figure 15. As an example, the TMS line connected to an IC in the I/O MCM slice is the "wired-OR" of the TMS lines of the two test buses JTAG1 and JTAG2 of Figure 15. Thus, if one TMS line is faulty, test control data can be sent over the other TMS line.

We now describe the test structures included in the four MCM slices. The test architecture for the processor MCM slice is shown in Figure 16.

The Local I/O chip (LIO) of the processor slice contains a JTAG Diagnostic Interface with provisons for a JTAG master controller and all JTAG bus signals. The LIO JTAG bus is controlled by the External Diagnostic Interface (COP) and the RAD6000 CPU through JTAG interface registers. Test data is placed on the LIO JTAG bus by the RAD60000 CPU directly or by an external source through the COP interface. Further, an additional JTAG bus (External JTAG) that can be controlled directly from an external source is provided. This enables direct and easy test access to the modules even when the JTAG Diagnostic Interface in the LIO is

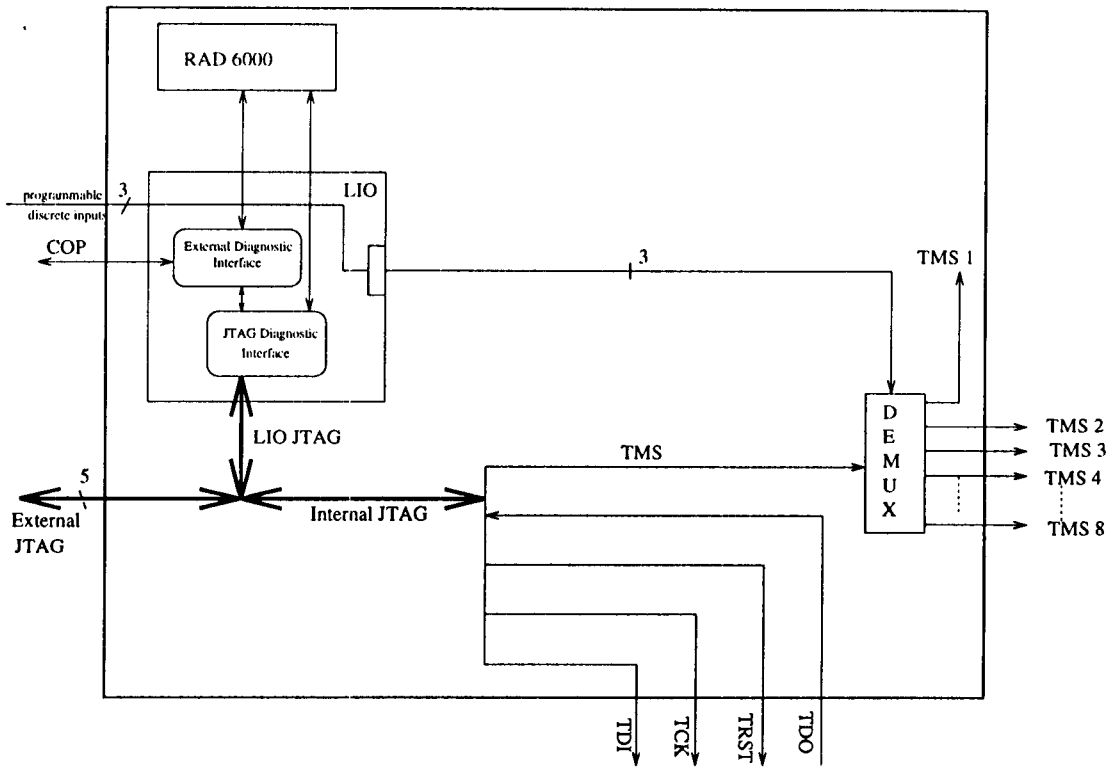

Figure 16: Test structures in the processor slice.

faulty. The External JTAG bus also enables direct observability of the test data being scanned by the RAD6000 CPU or the COP into the modules under test. Further, the External JTAG bus is used to test the JTAG diagnostic interface in the LIO, the RAD6000 JTAG interface, and the COP interface by scanning in the test data from either the COP or the processor into the external tester through the external JTAG bus. This allows diagnosis of faults in the test hardware of the processor MCM slice. The Internal JTAG bus is configured as the "wired-OR" of the External JTAG bus and the LIO JTAG bus as shown in the figure. Hence, while one JTAG bus (LIO or the External bus) is scanning in the test data into the slices, the other must be tri-stated. The DEMUX in the processor slice is controlled by the LIO chip.

The test structures for the other three modules are shown in Figures 17 through 19. The DRAM controller in the local memory MCM slice is JTAG compatible. Hence, test data is scanned into the controller and applied to the data and address buses of the memory stacks. A similar set up on the solid state recorder (SSR) module permits extensive test of its memory

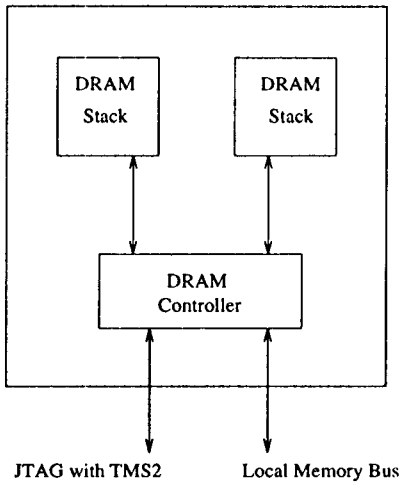

Figure 17: Test structures in the local memory slice.

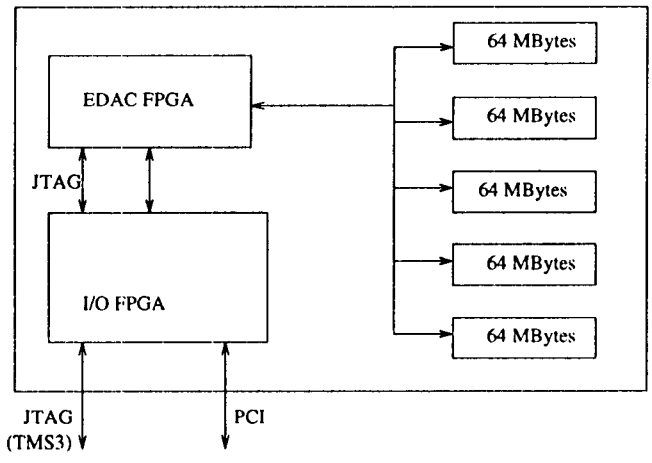

Figure 18: Test structures in the SSR slice.

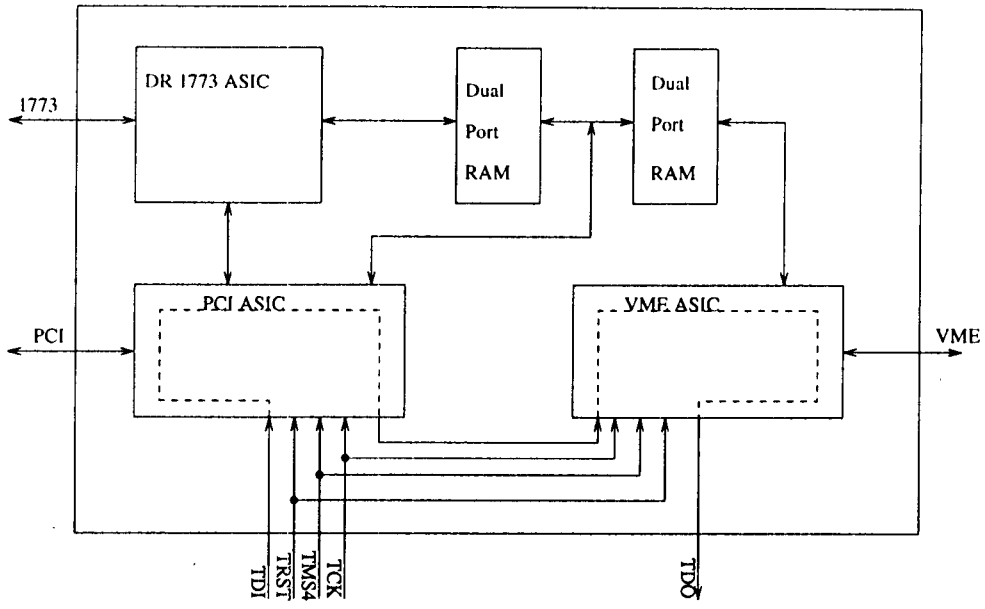

Figure 19: Test structures in the IO slice.

banks and FPGA controllers. The I/O module has a boundary scan chain through the PCI and VME controller ASICs. However, the DR 1773 ASIC is not JTAG compatible. The scan chain is shown in Figure 19. All the ASICs have Built In Selt Test (BIST) capability. The BIST test of the ASICs is enabled by the boundary scan RUNBIST instruction.

7 Test Procedure for NASAs 3D Microavionics Stack

The test procedure for NASAs 3D microavionics stack involves detailed test and diagnosis of the test architecture and MCM slices of the 3D stack as well as all interconnections concerned.

Initially, the JTAG test architecture of all the MCM slices is tested. This involves verifying the JTAG controllers and buses in all the slices. As the JTAG buses to all the slices are scanned out through the processor slice, it is essential that the JTAG Diagnostic Interface in the LIO is tested first. This involves testing the External JTAG bus, LIO JTAG bus, the COP interface, the RAD6000 CPU test interface and the DEMUX control. After the test architecture of the processor slice is validated, the test setup on the other slices is checked by scanning in serial data through the associated JTAG buses. This validates the correct functioning of the JTAG

test hardware in the 3D MCM stack.

Subsequently, the interconnections between the MCM slices of the 3D stack are tested. The PCI bus passing through all the modules and the memory data and address bus from the processor slice to the local memory slice are tested.

After all the interconnections between the stack slices are tested, the slices are tested individually. This process starts with exhaustive test of the processor MCM slice. The interconnections in the processor slice are tested first. Next, the RAD6000 CPU and the LIO IC are tested by enabling BS and BIST test, respectively. After, the processor slice is tested, the local memory slice is tested. This is followed by test of the SSR and I/O slices.

To generalize the above test procedure, consider that the test process can be described by a recursive algorithm as follows:

```
Test_Algorithm()
{
    1. Test the JTAG architecture of the 3D stack.
    2. Test(3D MCM Stack).
}

Test(Component)
{     Divide the Component into sub-Components.
    Test interconnections between the sub-Components.
    For all sub-Components do
       Test(sub-Component)
}
```

In the first iteration of the subroutine Test(), a Component corresponds to the entire 3D MCM stack. First, the interconnections between the MCM slices are tested. Then each slice is tested individually. When Test() is invoked again, a Component corresponds to an individual MCM slice. The sub-Components in this case are ICs in the MCM slice. The test flow diagram is shown in Figure 20. If a test fails at any step, then the external tester diagnoses the fault and repair is initiated. Subsequently, the complete test routine is repeated.

The proposed test structures have been fabricated and used to test NASAs 3D microavionics

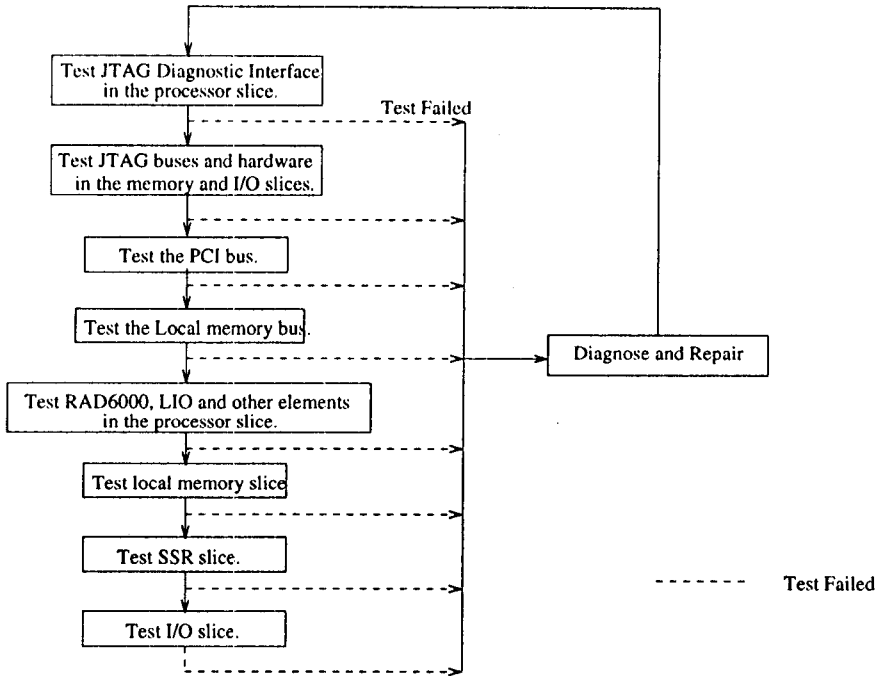

Figure 20: Test flow diagram for the 3D microavionics stack.

stack after assembly. While the spacecraft is in orbit, autonomous test of the stack can be initiated by the RAD6000 CPU. The test data and results, in this case, can be observed through the External JTAG bus and communicated to earth.

8 Conclusion

In this paper, we have presented test strategies for 3D MCM-based electronic systems. The test approaches have been analyzed and compared for test reliability and generalized so that test engineers can choose the test technique that best suits their requirements and constraints. Application of the proposed test techniques to test of NASAs 3D stack-based microavionics for the New Millennium Deep Space-1 mission is described. Methods for autonomous and reliable test of such 3D stacked MCMs have been proposed. It is seen that inclusion of these test techniques greatly enhances the ability and confidence of test engineers to test 3D MCM stacks in the presence of failures which can inhibit the operation of the test hardware itself and render the entire stack untestable. Such failures are of great concern in the fabrication of 3D MCM

stacks as opposed to MCMs themselves, due to the complexities of fabricating such stacks and the larger line lengths and mechanical stresses involved.

9 Acknowledgment

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